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# [[“]]SYSTEM FOR DRIVING COLUMNS OF A LIQUID CRYSTAL DISPLAY[[.”]]

~~DESCRIPTION~~

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## 1. Field of the Invention:

The present invention relates [[refers]] to a system for driving columns of a liquid crystal display.

## 2. Background of the Invention:

Liquid crystal displays (LCD) are used today in an ever-increasing number of products such as cellular telephones [[telephone]], portable computers, etc. The displays, which [[that]] can be in black and white, or in a grey or color [[colours]] scale, are usually made up of a matrix of electrodes in rows and columns. When driven by an appropriate voltage signal, a change in the optic behavior occurs at the crossing points of the rows and columns ("pixels"). ~~which, appropriately driven by means of the application of a voltage signal, cause at the crossing points, the so-called pixels, a change in optic behaviour of the liquid crystal placed between.~~

The image that is visualized on the display is obtained through different possible methods for driving the rows and the columns.

One method that is often used for driving an LCD [[and]] is known as Improved Alt & Pleshko (IA&P) and requires a single row electrode to be excited for an elementary period of time by [[means of]] a single selection pulse and the simultaneous excitation of the column electrodes. ~~; to the latter are then applied~~ Voltage [[voltage]] values are then applied to the column electrodes suitable for causing all the pixels that belong to that single row to be turned on or turned off. For a successive period of elementary time there is an [[will be the]] excitation of another row electrode and so on until the scanning of the last row electrode is completed; therefore if the row electrodes are a number N and T is the period of elementary time, the time needed for scanning all the rows will be given by NT which is also called a "frame".

The optic transmission characteristics of the liquid crystal vary with the amplitude of the voltage applied to the relative pixel, but the application of direct voltage is damaging to [[for]] the liquid crystal as it permanently changes and

degrades the physical properties of the material. For this reason, the voltage signals used to drive the single pixels of an LCD are alternating voltage in relation to a common value of direct voltage that is not necessarily [[has to be the]] ground potential. In this manner, the driving of a pixel of the display comes about through two waveforms of equal amplitude but with opposite polarity in relation to a common voltage, that follow each other periodically. Therefore the driving voltage applied to a given pixel during its period T within a frame is applied with opposite polarity during the respective period T of the successive frame.

Nevertheless, all these voltage transitions involve [[a]] significant power that has to be managed by the drive circuits. Therefore, one of the primary purposes in planning the LCD row and column driving devices [[of LCD rows and columns]] is to reduce the power consumption [[so as]] to minimize [[minimise]] both the power delivered by the power supplies of said devices, and the power dissipated by them.

One part of a driving device of LCD rows and columns, more precisely the Philips PCF8548 device, is shown [[described]] in Figure 1.

The LOW_FRAME signal is a logic signal that equals zero [[0]] in the even frames, and equals one [[1]] in the uneven frames. WHITE_PIX is [[instead]] a logic signal that equals zero [[0]] when the pixel is [[has to be]] on, and equals one [[equalling 1]] when the pixel is [[has to be kept]] off. Starting from these two signals are generated, through a circuit 1, the control signals that drive two PMOS transistors [[PMOS]] T9, T10 and two NMOS transistors [[NMOS]] T7, T8.

In particular, the gate terminals of [[the]] transistors T8, T9 and T10 are driven through 3 identical circuit cells C1, shown in Figure 2. Said cells are level-shifters, that is, buffers that convert the logic signal levels from a low voltage to a high voltage, in particular, from the supply voltage VDD to a driving voltage VLCD generated by a device (not shown in [[the]] Figure 2) comprising a booster regulator through the connection of a certain number of stages of a charge pump.

Each cell C1 comprises two NMOS transistors [[NMOS]] M22 and M23 driven by [[the]] signals A and NA, the output signal of the logic circuitry 1 and the negated signal A. The source terminals of [[the]] transistors M22 and M23 are coupled [[connected]] to the voltage VSS and the drain terminals are [[connected]] respectively coupled to the drain terminals of two PMOS transistors [[PMOS]] M20 and M21 on the source terminal of which the voltage VLCD is present; in addition the drain terminals of [[the]] transistors M22 and M23 are coupled [[connected]] to

the gate terminals of [[the]] transistors M21 and M20. The outputs Q drive the gate of [[the]] transistors T10, T9 and T8.

The gate terminal of [[the]] transistor T7 is [[instead]] driven directly by a logic low voltage signal.

The source terminal of the transistor T9 is connected to a voltage reference VA, while the drain terminal is coupled [[connected]] to the drain terminal of [[the]] transistor T10, whose source terminal is coupled [[connected]] to the voltage VLCD. The source terminal of [[the]] transistor T8 is coupled [[connected]] to a voltage reference VB, while the drain terminal is coupled [[connected]] to the drain terminal of [[the]] transistor T7, whose source terminal is coupled [[connected]] to the voltage VSS. The drain terminals of the pairs of transistor T7-T8 and T9-T10 are in common and supply the output signal OUT.

The voltages VA and VB are different levels of intermediate voltages between the voltages VLCD and VSS that are generated inside the drive device of an LCD. The relation between these levels and VLCD is chosen on the basis of the dimension of the matrix of the display according to the criteria that is [[will be]] shown and described below.

In particular, according to the technique of Improved Alt & Pleshko, to drive the liquid crystal display adequately, four different voltage levels intermediate between VLCD and VSS are generated inside the device. The relation between these and VLCD is set on the basis of the number of rows m of the display according to the relations:

VLCD, [(n+3)/(n+4)]*VLCD, [(n+2)/(n+4)]*VLCD, [2/(n+4)]*VLCD, [1/(n+4)]*VLCD, VSS)

with n given by $\sqrt{m - 3}$ [[the square root of m-3]].

If, for example, m = 81 => n = 6 in the case of a display with 81 rows the voltage levels will be:

VLCD (9/10)*VLCD (8/10)*VLCD (2/10)*VLCD (1/10)*VLCD VSS.

With reference to the drive circuit of Figure 1, in the case of a drive of columns, the voltage references VA and VB are [[will be]] equal respectively to (8/10)*VLCD and (2/10)*VLCD. The drive is provided [[will come about]], for example, in the following manner: in a frame [[the]] transistors T9 and T10 are [[will be]] turned on alternately, while transistors T7 and T8 are [[will be]] off; in this case

the output signal OUT, suitable for driving a column, varies [[will vary]] between VLCD and VA according to whether the corresponding pixel on the matrix of rows and columns given at the crossing point of the column and the row is on or not. In the successive frame [[the]] transistors T7 and T8 are [[will be]] turned on alternately, while [[the]] transistors T9 and T10 are [[will be]] off and therefore the output signal varies [[will vary]] between VSS and VB according to whether the pixel at [[of]] the crossing point of the corresponding column and row is [[will be]] on or not. The waveforms [[wave forms]] of the output signal OUT in the case of driving two columns COL0 and COL1 for a frame n and for the successive frame n+1 are shown in Figure 3. [[The]] Figure 4 shows the image as it appears on the display.

What is desired is [[In view of the state of the technique, the object of the present invention is to produce]] a system for driving columns of a liquid crystal display that has lower current [[minor]] consumption [[of current]] in comparison to known prior art devices.

## SUMMARY OF THE INVENTION

According to an embodiment of [[In accordance with]] the present invention, [[this object is achieved by means of]] a system for driving columns of a liquid crystal display includes [[comprising a]] logic circuitry operating in a supply path between a first and a second supply voltage with first said supply voltage higher than said second supply voltage, said logic circuitry being capable of generating starting from first logic signals in input second logic signals in output whose value is equal to said first or second supply voltage, elevator devices coupled to said logic circuitry and operating in a supply path between a third supply voltage greater than said first supply voltage and said second supply voltage, said elevator devices being capable of raising the value of said second logic signals, a first and a second pair of transistors having different supply paths and having an output terminal in common, said first and second pairs of transistors being associated to said elevator devices and to said logic circuitry so as to determine the drive signal of a column, wherein there are two [[characterised in that said]] elevator devices [[are two]] and each of them is coupled to [[connected with]] one of said pairs of transistors, and includes [[in that it comprises a]] turnoff circuitry coupled to said two elevator devices, said circuitry being capable of keeping one of the two pairs of transistors in the turnoff state in the period of time of a frame when the other of said two couples of transistors is [[in]]

operative [[conditions]].

## BRIEF DESCRIPTION OF THE DRAWINGS

The characteristics and the advantages of the present invention will appear evident from the following detailed description of an embodiment thereof illustrated as non-limiting example in the enclosed drawings, in which:

Figure 1 is a circuitry diagram of a driving device of columns of an LCD according to the known art;

Figure 2 is a more detailed circuitry diagram of a part of the circuit of Figure 1;

Figure 3 shows waveforms of the output voltage signal of the circuit of Figure 1 in the case of driving two columns;

Figure 4 shows an image formed on the display of an LCD;

Figure 5 is a circuitry diagram of a system for driving the columns of an LCD according to an embodiment of the invention;

Figure 6 is a more detailed circuitry diagram of the device of Figure 5; and

Figure 7 shows the temporal waveforms LOW_FRAME, WHITE_PIX, CN, CN_N, CP, CP_N and OUT concerning the circuit of Figure 6.

## DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Figure 5 shows a circuit diagram of a system for driving columns of an LCD according to an embodiment of the present invention. Said device comprises a low voltage logic circuit 10 operating between a supply voltage VDD and a supply voltage VSS, two level-shifters 11 and 12 operating between a supply voltage VLCD supplied by a device comprising a booster regulator through the connection of a certain number of stages of a charge pump (not shown in FIG. 5) and the voltage VSS, a pair of PMOS transistors [[PMOS]] T11, T12 and a pair of NMOS transistors [[NMOS]] T13, T14 having different supply paths. The principle on which the invention is based is that in a frame [[there will never be both the]] transistors PMOS T11, T12 or both [[the]] transistors NMOS T13, T14 are never both on. This permits the elimination of a level-shifter in relation to the drive device of Figure 1, as every level-shifter comprises in addition to the output signal its negated signal, but it is necessary to add [[a]] circuitry to keep the MOS transistors [[MOS]] not involved in the commutation during the abovementioned frame off; a decrease of the current used

in the drive device of the columns derives from this. Therefore the device of Figure 5 also comprises [[a]] turnoff circuitry 15 capable of generating two signals TR_STATE1 [[tr-state1]] and TR_STATE2 [[tr-state2]] suitable for turning off, alternately through [[the]] level-shifters 11 and 12, [[the]] PMOS transistors [[PMOS]] T11, T12 or [[the]] NMOS transistors [[NMOS]] T13, T14 not involved in the commutations with the succession of the frame.

The signal LOW_FRAME is a logic signal that equals zero [[0]] in the even frames, and equalling one [[1]] in the uneven frames. WHITE_PIX is [[instead]] a logic signal that equals zero [[0]] when the pixel has is [[to be]] on, and equalling one [[1]] when the pixel is [[has to be kept]] off. Starting from these two signals, through [[the]] circuit 10, the logic signals CP, CP_N, CN, CN_N, suitable for driving the level-shifters 11 and 12 are generated, which in turn drive PMOS [[the couple of]] transistors [[PMOS]] T11, T12 and NMOS [[the couple of]] transistors [[NMOS]] T13, T14.

Circuit [[The circuit]] 10 ensures that if the logic signal LOW_FRAME is at the one logic level [[1]], the signals CP and CP_N are placed at the zero logic level [[0]] and the signals CN and CN_N commutate following the commutation of the signal WHITE_PIX; more precisely, the signal CN is in phase with the signal WHITE_PIX while the signal CN_N is the signal CN negated.

Given that the logic signals CP and CP_N are at the zero logic level [[0]], the level-shifter 11 that is driven by said signals must be inactive so that PMOS [[the]] transistors [[PMOS]] T11 and T12 are off. In this case, the TR_STATE1 signal [[tr-state1]] generated by [[the]] circuitry 15 keeps [[the]] level-shifter 11 inactive. NMOS [[The]] transistors [[NMOS]] T13, T14 are driven by [[the]] level-shifter 12, which is operating and the output OUT of the column drive device varies between VSS and VB.

Again, [[the]] circuit 10 ensures that if the logic signal LOW_FRAME is at the zero logic level [[0]], the signals CN and CN_N are placed at the one logic level [[1]] and the signals CP and CP_N commutate following the commutations of the signal WHITE_PIX; more precisely the signal CP is in phase with the signal WHITE_PIX while the signal CP_N is the signal CP negated.

Given that the logic signals CN and CN_N are at the one logic level [[1]], [[the]] level-shifter 12 that is driven by said signals must be inactive so that NMOS [[the]] transistors [[NMOS]] T13 and T14 are off. In this case, the TR_STATE2

signal [[tr-state2]] generated by [[the]] circuitry 15 keeps [[the]] level-shifter 12 inactive. PMOS [[The]] transistors [[PMOS]] T11, T12 are driven by [[the]] level-shifter 11 operating and the output OUT of the column drive device varies between VLCD and VA.

Figure 7 shows the temporal diagrams of the signals LOW_FRAME, WHITE_PIX, CN, CN_N, CP, CP_N, OUT that derive from simulations relating to two successive frames, that is an even frame and an uneven frame.

Figure 6 shows the components of the column drive device of Figure 5 more in detail.

The low voltage logic circuitry 10 comprises several inverters as well as NAND and NOR gates [[NOT, NAND and NOR]] which, starting from the signals WHITE_PIX and LOW_FRAME in input to the circuitry 10 generate the logic signals CP, CP_N, CN, CN_N, suitable for driving [[the]] level-shifters 11 and 12 and having a voltage value equal to the voltage VDD or to the voltage VSS as shown in Figure 6.

Device [[The device]] 11 comprises two NMOS transistors [[NMOS]] M8 and M9 driven by the signals CP and CP_N, whose source terminals are coupled [[connected]] to the voltage VSS and whose drain terminals are coupled [[connected]] respectively to the drain terminals of two PMOS transistors [[PMOS]] M4 and M5 on the source terminal of which the voltage VLCD is present. The gate terminals of [[the]] transistors M4 and M5 are coupled [[connected]] to the drain terminals of [[the]] transistors M9 and M8.

The same drain terminals of [[the]] transistors M8 and M9 are coupled [[connected]] to the gate terminals of [[the]] transistors M2 and M1 on the source terminals of which the voltage VLCD is present, and at the drain terminals of [[the]] transistors M3 and M6 on the source terminals of which the voltage VLCD is present. Transistors [[The transistors]] M1, M2, M3, M6 belong to [[the]] turnoff circuitry 15 that also comprises a transistor M7 having its source terminal coupled [[connected]] to the voltage VSS, the drain terminal in common with the gate terminal of [[the]] transistors M3 and M6 and with the drain terminals of [[the]] transistors M1 and M2; the signal LOW_FRAME is present on the gate terminal.

Device [[The device]] 12 comprises two NMOS transistors [[NMOS]] M14 and M15 driven by the signals CN and CN_N whose source terminals are coupled [[connected]] to the voltage VSS and whose drain terminals are coupled [[connected]]

respectively to the drain terminals of two PMOS transistors [[PMOS]] M12 and M13 the gate terminals of which are coupled [[connected]] to the drain terminals of [[the]] transistors M15 and M14. The source terminals of [[the]] transistors M12 and M13 are coupled [[connected]] to the drain terminals of two transistors M10 and M11 having the gate terminals in common and the voltage VLCD is present on the source terminals. The gate terminal of [[the]] transistors M10 and M11 is connected to the gate terminal of [[the]] transistor M6.

The pair of PMOS transistors [[PMOS]] T11 and T12 has a supply path between the voltages VLCD and VA while NMOS [[the couple of]] transistors [[NMOS]] T13 and T14 has a supply path between the voltages VB and VSS. The gate terminals of [[the]] transistors T11 and T12 are coupled to [[connected with]] the drain terminals of [[the]] transistors M8 and M9 of [[the]] device 11, while the gate terminals of [[the]] transistors T13 and T14 are coupled [[connected]] with the drain terminals of [[the]] transistors M15 and M14 of [[the]] device 12. The common output terminal of [[the]] transistors T11 and T12 is coupled [[connected]] to the common output terminal of [[the]] transistors T13 and T14 and represents the output terminal OUT of the drive device of the present invention.

Circuit [[The circuit]] 10 ensures that, as [[it]] can be seen in Figure 6, if the logic signal LOW_FRAME is at the one logic level [[1]], the signals CP and CP_N are placed at the zero logic level [[0]] and the signals CN and CN_N commutate following the commutations of the signal WHITE_PIX; more precisely, the signal CN is in phase with the signal WHITE_PIX while the signal CN_N is the signal CN negated.

With the logic signals CP and CP_N at the zero logic level [[0]], [[the]] level-shifter 11 is inactive and PMOS [[the]] transistors [[PMOS]] T11 and T12 are off. In fact, [[the]] transistor M7 is on and causes [[the]] transistors M3 and M6 to turn on as it brings the voltage on their gate terminals at VSS; in this manner, the voltage on the gate terminals of the transistors T11 and T12 is brought to a voltage that is substantially the same as VLCD by [[means of the]] transistors M3 and M6. The turning on of [[the]] transistor M7 causes [[the]] transistors M10 and M11 to turn on, bringing the voltage on the source terminals of [[the]] transistors M12 and M13 substantially [[practically]] the same as VLCD. In this case, the TR_STATE1 signal [[tr-state1]] generated by circuitry 15 is high and keeps [[the]] level-shifter 11 inactive; the TR_STATE2 signal [[tr-state2]] is low and permits [[the]] device 12 to

turn on. The NMOS transistors [[NMOS]] T13, T14 are driven by [[the]] level-shifter 12 operating and the output OUT of the column drive device varies between VSS and VB.

Again, [[the]] circuit 10 ensures that if the logic signal LOW_FRAME is at the zero logic level [[0]], the signals CN and CN_N are placed at the one logic level [[1]] and the signals CP and CP_N commutate following the commutations of the signal WHITE_PIX; more precisely, the signal CP is in phase with the signal WHITE_PIX while the signal CP_N is the signal CP negated.

With the logic signals CN and CN_N at the one logic level [[1]], [[the]] level-shifter 12 is inactive and NMOS [[the]] transistors [[NMOS]] T13 and T14 are off. In fact, [[the]] transistor M7 is off and the turning on of one of [[the]] transistors M8 or M9 causes one of [[the]] transistors M2 or [[o]] M1 to turn on as it brings the voltage on their gate terminals to VSS; in this manner, the voltage on one of the gate terminals of [[the]] transistors T11 and T12 is brought to a voltage which is substantially equal to VSS. The turning on of one of [[the]] transistors M1 or M2 causes [[the]] transistors M3 and M6 to turn off and [[the]] transistors M10 and M11 that inhibit the turning on of [[the]] device 12 and of [[the]] transistors T13 and T14 to turn off. In this case, the TR_STATE2 signal [[tr-state2]] generated by [[the]] circuitry 15 is high and keeps [[the]] level-shifter 12 inactive; the TR_STATE1 signal [[tr-state1]] is low and permits [[the]] device 11 to turn on. The PMOS transistors [[PMOS]] T11, T12 are driven by [[the]] level-shifter 11 operating and the output OUT of the column drive device varies between VLCD and VA.

While there have been described above the principles of the present invention in conjunction with a specific circuit and timing implementation it is to be clearly understood that the foregoing description is made only by way of example and not as a limitation to the scope of the invention. Particularly, it is recognized that the teachings of the foregoing disclosure will suggest other modifications to those persons skilled in the relevant art. Such modifications may involve other features which are already known per se and which may be used instead of or in addition to features already described herein. Although claims have been formulated in this application to particular combinations of features, it should be understood that the scope of the disclosure herein also includes any novel feature or any novel combination of features disclosed either explicitly or implicitly or any generalization or modification thereof which would be apparent to persons skilled in the relevant art,

whether or not such relates to the same invention as presently claimed in any claim and whether or not it mitigates any or all of the same technical problems as confronted by the present invention. The applicants hereby reserve the right to formulate new claims to such features and/or combinations of such features during the prosecution of the present application or of any further application derived therefrom.